Fermi National Accelerator Laboratory

SVX II Silicon Strip Detector Upgrade Project

Readout Electronics

SVX III Detector Emulator Module

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1. GENERAL INFORMATION

The SVX III Detector Emulator Module is a test-stand-only device implemented as a VIPA 9U Transition Module. Its purpose is to provide a single FIB module with data which follows the protocol defined for the SVX III ASIC. Under control of data values written to it by the FIB the SVX III Detector Emulator Module provides variable amounts of data in either fixed, pseudo-random, or fully random patterns. Certain error conditions may

also be created on demand in order to test system software response.

As a secondary feature the Detector Emulator Module provides partial emulation of a second Port Card such that diagnostic software may determine what DDR commands were actually sent by the FIB during a readout sequence.

1.1. Description Of Component & How It Fits Into The System

The SVX III Detector Emulator Module fits into the system only during system startup and integration. It is not meant for use in the delivered system and is inappropriate for use outside the engineering development area. No user-level software is provided for the device. The SVX III Detector Emulator Module is not guaranteed to provide timing identical to that of the SVX III chip/Port Card combination. The Detector Emulator Module is only useful for checking the response of the system to data conditions and for engineering analysis of setup and hold times within modules.

1.2. List Of Component Requirements

For operation the SVX III Detector Emulator Module requires a FIB module and a VIPA subrack. Power for the module is provided by the subrack, and necessary control information is provided by the FIB. The VIPA subrack must be outfitted with a J3 backplane for command and data connection.

2. THEORY OF OPERATION AND OPERATING MODES

2.1. Basic Features & Operation (Including Block Diagram)

The SVX III Detector Emulator Module delivers SVX-like data to all 10 pipeline processors of the FIB, plus optional connection to either the copper or optical FIB Transition Module as shown in Figure 1. The user may select various operational features by programming the control bits in the control latch. Having specified the operational characteristics of the Detector Emulator Module, the FIB is then programmed to issue Back-end clocks. The parallel and identical state machines create identical data patterns in all twelve output registers.

Ten of the registers feed directly back into the FIB to exercise all ten pipeline processors. An additional two outputs allow for connection to either a Copper FIB Transition Module or an Optical FIB Transition Module for loopback testing of a single channel of either. The Copper FIB Transition Module is driven directly with a cable. Provision is given for the insertion of a DOIM Transmitter daughter card, identical to the DOIM board used with the BERT. This allows testing of one DOIM link back to the Optical FIB Transition Module.

The Detector Emulator Module responds to Port Card commands driven by the FIB. Commands sent from the FIB to Port Card ‘A’ are merely recorded by the Detector Emulator Module and played back as the status values of SVX data (if the user sets the appropriate control bit) in response to Back-end clocks. This allows system software to verify that the correct DDR commands have been issued by the FIB prior to readout. Section 4 details which DDR commands are mapped to the status bits as data is generated.

Writes to Port Card ‘B’ are interpreted by the Detector Emulator Module as configuration commands. Unlike the connection to Port Card ‘A’, the control interface of the Detector Emulator Module is completely different than that of the Port Card. The most significant function address (C5), plus the control bit C_DATA, are used as a register select pair. With each command write to Port Card ‘B’, five bits of Detector Emulator Module configuration data are written to one of four configuration registers, allowing a total of 20 Detector Emulator Module configuration bits. These bits are allocated as:

- 4 bits for the Number Of Chips to emulate (NCHIPS)
- 7 bits for the Number of Words Per Chip (NWORDS)

- 7 bits for Detector Emulator Module Control Functions (RAND_EN, VAR_DATA, ID_SEL, NULL_SEL, DATA_TYPE, BE_INHIBIT and STAT_INHIBIT)
- 2 Spare bits reserved for future use.

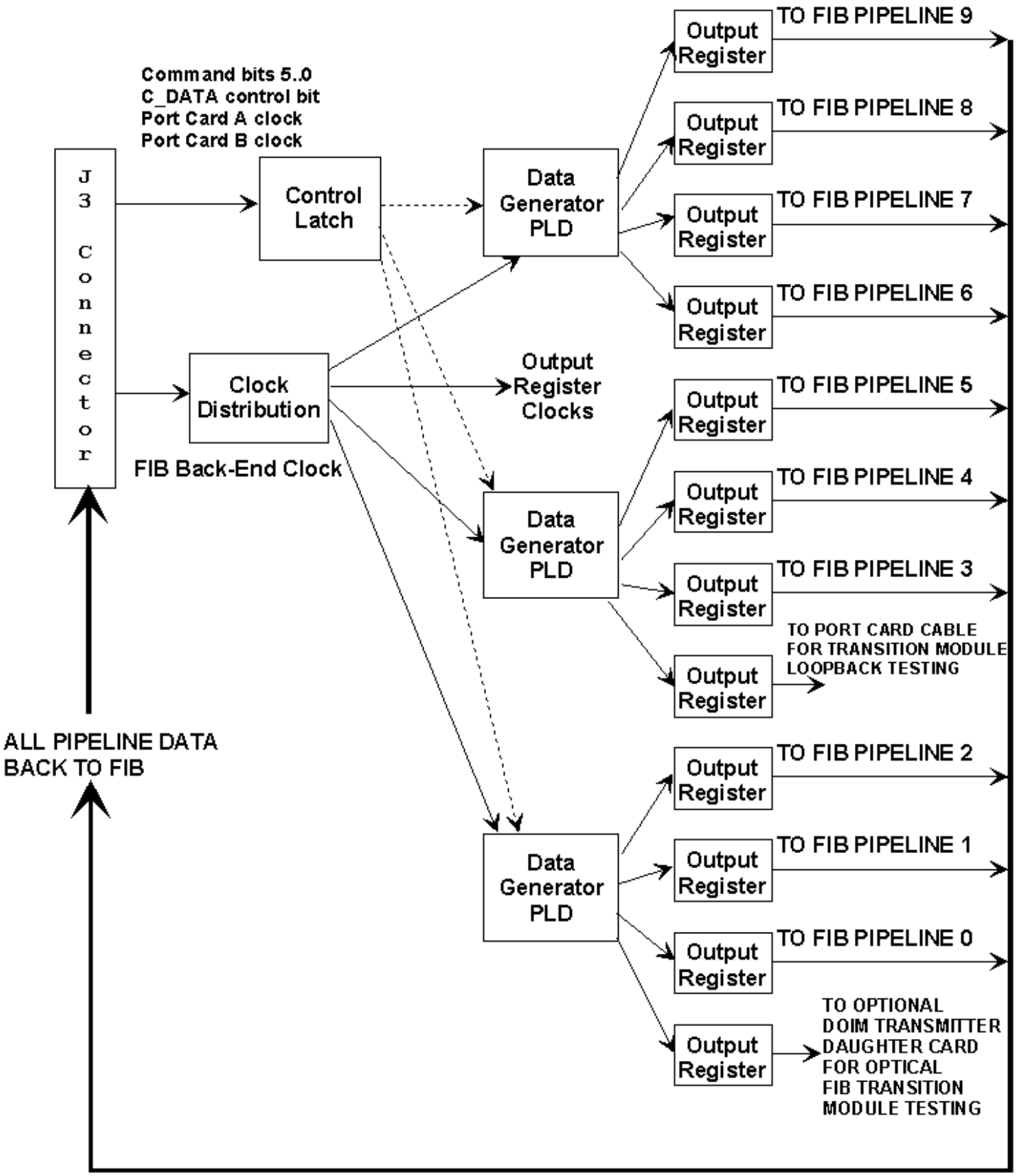


Figure 1

Block Diagram of Detector Emulator Module

The normal response of the Detector Emulator Module to Back-end clocks is to present NCHIPS worth of data, where each of the chips issues NWORDS of data. Each data value is presented along with an address, and each chip is prefaced by a Chip ID and a Status value, such that the amount of data generated in the default mode is given by Equation 1.

$$\#bytes = \left[(NWORDS * 2) + 2 \right] * NCHIPS$$

Equation 1

Formula for Amount of Data Generated by Detector Emulator Module in Basic Mode

This default number of bytes can range from a minimum of four (one chip, only one word for that chip) to a maximum of 4,128 bytes (128 words per chip, times sixteen chips). Back-end clocks in excess of that required to issue the programmed amount of data are ignored as the internal state machine enters a 'null' state after all data requested has been issued. Insufficient back-end clocks will merely cause the internal state machine to halt at that point.

2.2. Standard Detector Emulator Module Data Format

The normal output data format of the Detector Emulator Module looks like SVX data. Eight-bit data values are generated with an Odd Byte Data Valid bit as given in Table 1.

CHIP ID	**1**
STATUS WORD	**0**
ADDRESS	**1**
DATA	**0**
ADDRESS	**1**
DATA	**0**
…	**…**
…	**…**

CHIP ID	**1**
STATUS WORD	**0**
ADDRESS	**1**
DATA	**0**
…	**…**
…	**…**

Table 1

Basic SVX Data Format Including OBDV State

Data is issued as one continuous stream. Chip ID and Status values have the most significant bit set, whereas Address and Data values do not. Chip ID values normally decrement during readout with the last Chip ID being zero. Bit 5 in the Chip ID byte is set is addition to the most significant bit (bit 7) for the last half of chips being emulated. For example, if the control registers were configured for 8 chip emulation, the Chip ID byte of the data stream would follow the sequence shown in Table 2.

Chip ID	Chip ID byte
7	0x87
6	0x86
5	0x85

4	0x84
3	0xA3
2	0xA2
1	0xA1
0	0xA0

Table 2

Chip ID Byte Format for 8 Chip Emulation

If the STAT_IHIB control bit is set, the status byte is always 0x80, otherwise the Status Word is indeterminate as it is dependent upon the DDR control values written by the FIB to Port Card ‘A’.

The Address values increment with the last Address being 0x7F. The Data values normally decrement (unless is pseudo or fully random mode) with the last value also being 0x7F.

Setting of the Detector Emulator Module control bits may change the rules regarding the order of Chip ID values and the Data Values. However, the Address values always follow the incrementing rule given here, and the number of Data words is always constrained to be less than or equal to 128. Also, the use of the MSB to indicate Chip ID/Status versus Address/Data is inviolate.

3. **Effect of RAND_EN control bit**

When the RAND_EN bit is set, the data bytes are random. Data is generated from a 38 bit LFSR in each data generator. The LFSR uses the 53MHz MCLK from the backplane as its clock source to generate a pattern that will repeat itself every ~90min. The random seed is the time between the start of MCLK (starts at power up) and the start of the first data stream the DEM sends. Since this time depends on human interaction time with the test stand software, it not a repeatable seed resulting in different data each run. Note that while the data is random, data across all channels should be the same.

2.4. Effect of the VAR_DATA control bit

If the VAR_DATA bit is set, the amount of data generated by the Detector Emulator Module is pseudo-random but guaranteed not to exceed 258 bytes per chip. In this mode of operation, the number of words generated per chip is a function of the original requested NWORDS and the current Chip ID value as shown in Equation 2. The purpose of VAR_DATA is to allow the Detector Emulator Module to provide variant amounts of information to exercise system timing and readout buffer handling.

$$\begin{aligned} NewNWORDS = {} & (NWORDS[5]*64) \\ & +(CHIPID[3]*32) \\ & +(CHIPID[1]*16) \\ & +(CHIPID[2]*8) \\ & +(CHIPID[0]*4) \\ & +(NWORDS[3]*2) \\ & +NWORDS[1] \end{aligned}$$

Equation 2

Calculation of Amount of Data Generated in VAR_DATA Mode

Since each successive chip has a different ID value, the number of bytes of data will be different for each chip. As an example, if a data pattern with 16 chips is programmed, with a requested number of words equal to 6 words per chip, the Detector Emulator Module will generate (with VAR_DATA set), the following pseudo-random NWORDS settings:

Chip ID	Pseudo-Random NWORDS value
15	61
14	57
13	45
12	41
11	53
10	49
9	37
8	33
7	29
6	25
5	13
4	9

3	21
2	17
1	5
0	1

Table 3

Example of VAR_DATA Effect

2.5. Effect of the DATA_TYPE control bit

The DATA_TYPE control bit modifies the outuput data values without changing the amount of data presented by the Detector Emulator Module. If DATA_TYPE is set, a series of exclusive-OR gates changes the Data values. The nominal equation (with DATA_TYPE not set) is

$$Data = \overline{Address} - 1$$

with the MSB = 0 such that the typical data output decrements with each successive word. When DATA_TYPE is set, the output data changes according to the following formula:

DATA[7] = 0

DATA[6] = ADDR[5] $!ADDR[3];

DATA[5] = ADDR[4] $!ADDR[0];

DATA[4] = ADDR[3] $!ADDR[4];

DATA[3] = ADDR[2] $!ADDR[5];

DATA[2] = ADDR[1] $!ADDR[6];

DATA[1] = ADDR[0] $!ADDR[1];

DATA[0] = !ADDR[4] $ ADDR[2];

where the '$' indicates the exclusive-OR function. A typical data output when DATA_TYPE is set is shown in Table 3. DATA_TYPE is useful for exercising data-value dependent system functions such as the pedestal and gain correction features of the FIB.

ADDR	DATA
0x76	0x0D
0x77	0x2F
0x78	0x52

0x79	0x70
0x7A	0x54
0x7B	0x76
0x7C	0x7B
0x7D	0x79
0x7E	0x5D
0x7F	0x7F

Table 4

Typical Output When DATA_TYPE is Set

2.6. Effect of the ID_SEL Control Bit

The ID_SEL control bit, when set, overrides the normal, rational set of Chip ID values with a pseudo-random sequence. This feature is useful for checking the 'last Chip ID' recognition circuit of the FIB and for exercising system software which should monitor the Chip ID values. When ID_SEL is set, the internal CHIP_ID count is replaced by the following equation set:

CHIP_ID3 = CCNT1;

CHIP_ID2 = !CCNT0;

CHIP_ID1 = !CCNT2;

CHIP_ID0 = CCNT3;

This results in the mapping shown in Table 4. All Chip ID values are still presented, and all are unique, but the order is scrambled. The FIB is normally programmed to stop collecting data after a certain Chip ID value has been seen (usually Chip ID 0), so it is possible for the data record as read from the FIB to be truncated with respect to the amount of data requested when ID_SEL is set.

CHIP ID (Normal)	CHIP ID (ID_SEL set)
0	6
1	2
2	14

3	10
4	4
5	0
6	12
7	8
8	7
9	3
10	15
11	11
12	5
13	1
14	13
15	9

Table 5

Effect of ID_SEL bit on Chip ID Values

2.7. Effect of the NULL-SEL bit

The NULL_SEL bit, if set, merely changes the number of null, or empty, cycles between chips from two clocks to one. It is used to test the internal operations of the FIB and should not in any way affect the data seen at the output of the FIB or at the output of the VRB.

2.8. Effect of the BE_INHIBIT bit

The BE_INHIBIT bit, if set, makes the response of the Detector Emulator Module to the Back-end clock dependent on the DDR setups written by the FIB to the Port Card ‘A’ interface. Specifically, the two mode control functions (FE_MODE, DDR command 18 and BE_MODE, DDR command 19) are monitored to determine which of the four SVX operational modes the FIB has requested. Response to the Back-end clock is inhibited if the selected mode is not Readout (FE_MODE == 1 and BE_MODE == 0).

9. **Effect of the STAT_INHIB bit**

With STAT_IHIB control bit set, the status byte (immediately follows Chip ID) is always x80. If this control bit is not set, the value of the status byte is more complex. When STAT_IHIB = 0 the DEM provides feedback, through the Status words, of what commands the FIB sent to the DDR. This is accomplished by providing a bitmap scattered across four Status words which shows which DDR functions were enabled or disabled by the FIB. In the Port Card/DDR interface, the FIB command bits C0..C4 select a DDR function. The DDR function is enabled by selecting a particular function and writing to it with the C_DATA bit set. To disable a function, the same address is selected and the C_DATA bit is not set.

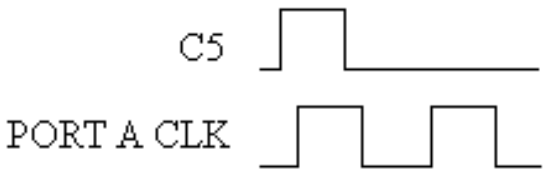
The Detector Emulator Module stores the state of the C_DATA bit for each of the 32 possible DDR functions, with the exception of function zero (Port Card Reset). When data is read back from the Detector Emulator Module, the status of the defined DDR functions is read back as the low seven bits of the Status value (only when STAT_IHIB = 0). Which seven of the 31 DDR functions are read back is determined by the two least significant bits of the Chip ID, such that reading out four chips of data gives all the DDR information. Should the FIB issue a Port Card Reset command (function zero), all Status readback values are reset to zero.

The intended purpose of the Status function is to monitor the DDR commands sent by the FIB during the Digitize and Readout operations.

2.10. Usage Instructions

The user sets up the operation of the Detector Emulator Module by performing the following sequence:

1. Apply power.
2. Write four command words to the Detector Emulator Module via the Port Card ‘B’ interface to set programmable functions. Six writes are required as the FIB may only set five bits with each write. The remaining two bits of the FIB command word are used to select which of four sets of five command bits are overwritten.



3. Perform Port Card (DDR) initialization and setup to Port Card ‘A’. In order for the DEM data generators to receive the proper reset, the C5 bit must be asserted and at least two Port Card ‘A’ clocks issued. This pattern should be present at then end of each DDR initialization:

4. Issue Back-End clocks to obtain data. The Detector Emulator Module is fully synchronous and creates no output unless Back-End clocks are applied.

2.11. Hardware Diagnostic Features

The Detector Emulator Module also provides headers for access to the J3 Backplane command bus to facilitate testing of FIB Fanout to FIB communication. Connection points are provided for interface to a DOIM transmitter to allow future use of the Detector Emulator Module to exercise the optical version of the FIB Transition Module.

All logic in the Detector Emulator Module is implemented in In-System Programmable logic to allow field upgrades and simplified testing.

3. INTERFACE SPECIFICATIONS

The Detector Emulator Module is directly connected to the FIB J3 connector for commands and clocks. The data generated by the Detector Emulator Module is directly driven to the J3 connector of the FIB. All signal levels are TTL. The power for the Detector Emulator Module is derived from the J0 connector of the VIPA backplane. Only +5 volts is used.

3.1. Internal Control Registers (Port Card 'B')

Four registers are implemented inside the Detector Emulator Module. The user selects which register is written to by using the C_DATA and C5 bits as a two bit selection code. The selection is asynchronously decoded and the rising edge of the CMD_CLOCK is used to register the data values. One 53 MHz clock cycle should provide sufficient setup time. Each of the four 5-bit-wide registers is detailed below.

FIB Command Bit (as sent to Port Card)	Detector Emulator Module Function
0-3 (NCHIPS)	Sets Number of Chips worth of data sent. (1-15 give 1-15 chips worth, zero gives 16 chips worth)
4 (RAND_EN)	1: Fully random data. 0: Normal or Pseudo random data.

Table 6

Detector Emulator Module Register 0 (C_DATA = 0, C5 = 0)

FIB Command Bit (as sent to Port Card)	Detector Emulator Module Function
0 (VAR_DATA)	1: Allows variable data length per chip. 0: Fixed amount of data per chip as set by NWORDS value.
1 (ID_SEL)	1: Chip ID's follow pseudo-random sequence. 0: Chip ID's are simple binary count.
2 (NULL_SEL)	1: One null cycle between chips. 0: Two null cycles between chips.

3 (DATA_TYPE)	1: Channel data follows pseudo-random pattern. 0: Normal data.
4 (SPARE1)	No function.

Table 7

Detector Emulator Module Register 1 (C_DATA = 0, C5 = 1)

FIB Command Bit (as sent to Port Card)	Detector Emulator Module Function
0-4 (NWORDS[4..0])	Bits 0..4 (least significant) of seven-bit Number of Words control value.

Table 8

Detector Emulator Module Register 2 (C_DATA = 1, C5 = 0)

FIB Command Bit (as sent to Port Card)	Detector Emulator Module Function
0-1 (NWORDS[6..5])	Bits 5,6 (most significant) of seven-bit Number of Words control value.
2 (STAT_INHIB)	When set, status byte is always 0x80, otherwise status byte is a function of DDR writes.
3 (SPARE 2)	No function.
4 (BE_IHNIB)	If set, forces device to only issue data in response to Back-end clocks if SVX mode is Readout. If clear, device always issues data in response to Back-end clock.

Table 9

Detector Emulator Module Register 3 (C_DATA = 1, C5 = 1)

3.2. DDR Command Readback Format (Port Card ‘A’)

The two least significant bits of the Chip ID counter are used to select one of four seven-bit values which are read back as the least significant seven bits of the status word. 31 possible DDR command functions exist, with DDR command 0 reserved for "Port Card reset". Inside the Detector Emulator Module, 31 D flip flops are implemented which load the state of C_DATA for each of the possible command function values. Selection of command 0 (reset) asynchronously resets all 31 flip-flops to zero. Thus, when reading the status words generated by the

Detector Emulator Module, any 1's in the status word indicate DDR functions which have been set by the FIB since the last Port Card reset. Zeroes indicate either functions which have not been set since the last reset, or functions which have been explicitly reset by the FIB since the last read.

The DDR documentation as of May 8, 1997 lists the command numbers as having the following interpretation:

C[0:4]	NAME	Description
0	RESET	Reset/preset the FFs of the control lines of the SVX3 chips
1	DDR1	Enable DDR1 chip
2	DDR2	Enable DDR2 chip
3	DDR3	Enable DDR3 chip
4	DDR4	Enable DDR4 chip
5	DDR5	Enable DDR5 chip
6	SVX3_RB	Enable SVX3 Readback on BUS0
7	DAC0	DAC0 Value
8	DAC1	DAC1 Value
9	DAC2	DAC2 Value
10	DAC3	DAC3 Value
11		Available
12		Available
13	SEL0	Multiplexer output select 0
14	SEL1	Multiplexer output select 1
15	V2_EN	Enable voltage regulator 2
16	NOP	No Operation
17	CH_MODE	Change Mode signal for SVX3 chips
18	FE_MODE	Front End Mode signal for SVX3 chips
19	BE_MODE	Back End Mode signal for SVX3 chips
20	CAL_SR	Calibration inject, Strobe signal for SVX3 chips
21	PIPE_RD1	PIPE-RD1 signal for SVX3 chips

22	PA_RST	Pre-amplifier reset
23	COMP_RST	Comparator Reset (BUS0) signal for SVX3 chips
24	RAMP_RST	Ramp Reset (BUS1) signal for SVX3 chips
25	CNTR_RST	Counter Reset (BUS2) signal for SVX3 chips
26	RREF_RST	Ramp Reference Reset signal(BUS3) for SVX3 chips
27	TN	Top Neighbor signal for SVX3 chips
28	BUF_EN	Tri state control for BUS[0:3]
29		Available
30	DRV_EN	Driver enable (enables the TX-DOIM outputs)
31	V1_EN	Enable voltage regulator 1

Table 10

DDR Command Codes as taken from DDR specification

3.2.1. Organization of DDR Commands into the Status words

To compact the data into four 7-bit values, the flip-flops for commands 29, 16, 12 and 11 have been ignored. This leaves 27 status bits which are read out over four status values. The low 2 bits of the Chip ID are used to select which set of command status bits are provided as given in Tables 10 through 13.

The actual Chip ID as presented in the data is used as the table index. Software should use the Chip ID value as read in order to interpret the immediately following Status word.

Status Bit	DDR Function Number	Meaning if set (bit = 1)	Meaning if clear (bit = 0)
STAT6	31	voltage regulator 1 enabled	voltage regulator 1 disabled
STAT5	30	TX-DOIM enabled	TX-DOIM disabled
STAT4	28	Readback 3-state buffer enabled	Readback 3-state buffer disabled
STAT3	27	TN bit set	TN bit clear
STAT2	26	Ramp Reference Reset bit set	Ramp Reference Reset bit clear

STAT1	25	Counter Reset bit set	Counter Reset bit clear
STAT0	24	Ramp Reset bit set	Ramp Reset bit clear

Table 11

Interpretation of Status Bits for Chip ID values 0,4,8,12

Status Bit	DDR Function Number	Meaning if set (bit = 1)	Meaning if clear (bit = 0)
STAT6	23	Comparator Reset bit set	Comparator Reset bit clear
STAT5	22	Preamp Reset bit set	Preamp Reset bit clear
STAT4	21	PIPE-RD1 bit set	PIPE-RD1 bit clear
STAT3	20	CAL INJ bit set	CAL INJ bit clear
STAT2	19	Back End Mode bit set	Back End Mode bit clear
STAT1	18	Front End Mode bit set	Front End Mode bit clear
STAT0	17	Change Mode bit set	Change Mode bit clear

Table 12

Interpretation of Status Bits for Chip ID values 1,5,9,13

Status Bit	DDR Function Number	Meaning if set (bit = 1)	Meaning if clear (bit = 0)
STAT6	15	Voltage Regulator 2 enabled	Voltage Regulator 2 disabled
STAT5	14	Multiplexer select 1 set	Multiplexer select 1 clear
STAT4	13	Multiplexer select 0 set	Multiplexer select 0 clear
STAT3	10	DAC3 bit set	DAC3 bit clear
STAT2	9	DAC2 bit set	DAC2 bit clear
STAT1	8	DAC1 bit set	DAC1 bit clear
STAT0	7	DAC0 bit set	DAC0 bit clear

Table 13

Interpretation of Status Bits for Chip ID values 2,6,10,14

Status Bit	DDR Function Number	Meaning if set (bit = 1)	Meaning if clear (bit = 0)
STAT6	6	SVX readback on BUS0 enabled	SVX readback on BUS0 disabled
STAT5	5	DDR5 enabled	DDR5 disabled
STAT4	4	DDR4 enabled	DDR4 disabled
STAT3	3	DDR3 enabled	DDR3 disabled
STAT2	2	DDR2 enabled	DDR2 disabled
STAT1	1	DDR1 enabled	DDR1 disabled
STAT0	N/A	N/A	Always reads zero

Table 14

Interpretation of Status Bits for Chip ID values 3,7,11,15

With the exception of the interpretation of the operational mode enabled by the BE_INHIBIT control, none of the Status bit values in any way affect the data presented by the Detector Emulator Module. There is no emulation of analog conversion functions such as Preamp Reset. In the real SVX system these bits need to be set from time to time to insure proper analog operation of the converter. When using the Detector Emulator Module, software may require that these bits read back ‘1’ every so many events in order to emulate the same analog functionality. However, to insure that Detector Emulator Module data is meaningful for all events, no attempts have been made to emulate analog conditions.

4. ELECTRICAL & MECHANICAL SPECIFICATIONS

Mechanically compliant with VIPA 9U X 120 mm Transition Module format. Power dissipation of less than 4 Amps of +5 volts, total under 20 Watts. +5 volt power is taken from the J0 connector.

5. SAFETY FEATURES & QUALITY ASSURANCE PROCEDURES

Not safe for use by physicists, scientists, programmers or management without the supervision of a trained technician or engineer. Proper construction techniques for multilayer circuit boards including solid power and ground planes, sufficient decoupling, fusing and transient suppression are followed.